Reliability Test Report

Product Name: CA-IS37XX

Report Version: V1.4

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1. Overview

Reliability testing of microelectronic products is a risk mitigation process designed to ensure the service life of device in customer applications. Semiconductor wafer manufacturing process and package-level reliability can be assessed in a variety of ways and may include accelerated environmental test conditions. Chipanalog evaluates manufacturability of the device to verify a robust silicon and assembly flow to ensure continuity of supply to customers. Chipanalog qualifies new devices, significant changes, and product families based on JEDEC JESD47. CA-IS37XX series chips are packaged with the same wafer. The differences between part numbers are the package and bonding diagram. The data shown is representative of the material sets, processes, and manufacturing sites used by the device family

2. Part Number List

Package Type	**Part Number**
SOIC16-WB(W)	CA-IS3720HW/CA-IS3721HW/CA-IS3722HW/CA-IS3720LW/CA-IS3721LW/CA-IS3722LW CA-IS3730HW/CA-IS3731HW/CA-IS3730LW/CA-IS3731LW CA-IS3740HW/CA-IS3741HW/CA-IS3742HW/CA-IS3740LW/CA-IS3741LW/CA-IS3742LW CA-IS3760HW/CA-IS3761HW/CA-IS3762HW/CA-IS3763HW/CA-IS3760LW/ CA-IS3761LW/CA-IS3762LW/CA-IS3763LW
SOIC16-NB(N)	CA-IS3730HN/CA-IS3731HN/CA-IS3730LN/CA-IS3731LN CA-IS3740HN/CA-IS3741HN/CA-IS3742HN/CA-IS3740LN/CA-IS3741LN/CA-IS3742LN CA-IS3760HN/CA-IS3761HN/CA-IS3762HN/CA-IS3763HN/CA-IS3760LN/ CA-IS3761LN/CA-IS3762LN/CA-IS3763LN
SSOP16(B)	CA-IS3731HB/ CA-IS3731LB/ CA-IS3740HB/CA-IS3740LB/CA-IS3741LB/ CA-IS3741HB/ CA-IS3742HB/ CA-IS3742LB

Note: JEDEC specification is designed to also qualify a family of similar components utilizing the same fabrication process, design rules, and similar circuits. The family qualification may also be applied to a package family where the construction is the same and only the size and number of leads differs.

3. Product Information

3.1. Wafer Information

Wafer	ZHUQUE_P	ZHUQUE _S
Fab Process	18BCD	18BCD

3.2. Package Information

Assembly site	SFA/SiMAT/UNIMOS/JCET	SFA/SiMAT/JCET	池州华宇/JCET
FT site	SFA/SiMAT/UNIMOS/JCET	SFA/SiMAT/JCET	池州华宇/JCET
Package	SOIC16-WB	SOIC16-NB	SSOP16
Lead frame	Cu	Cu	Cu
Bond wire	20um Au	20um Au	20um Au
MSL level	MSL3	MSL3	MSL3

4. Reliability Qualification Plan

4.1. Device Qualification Test Requirements

Stress	Ref.	Abbv.	Conditions	Duration /Accept
Electrical Parameter Assessment	JESD86	ED	Per Datasheet	Per Datasheet
High Temperature Operating Life	JESD22-A108, JESD85	HTOL	$T_J \geq 125°C$ $V_{CC} \geq V_{CC}$ max	1000 hrs/0 Fail
Human Body Model ESD	JS-001	ESD-HBM	$T_A = 25°C$	Classification
Charged Device Model ESD	JS-002	ESD-CDM	$T_A = 25°C$	Classification
Latch-Up	JESD78	LU	Class I or Class II	Classification

4.2. Nonhermetic Package Qualification Test Requirements

Stress	Ref.	Abbv.	Conditions	Duration /Accept
MSL Preconditioning	JESD22-A113	PC	Per appropriate MSL level per J-STD-020	Electrical Test (optional)
High Temperature Storage	JESD22-A103 & A113	HTSL	150°C, 1000 hrs	1000 hrs/0 Fail
Temperature Humidity Bias	JESD22-A101	THB	85°C, 85% RH, V_{CC} max	1000 hrs/0 Fail
Highly Accelerated Temperature and Humidity Stress	JESD22-A110	HAST	130°C/110°C, 85% RH, V_{cc1}= 5.5V, V_{cc2}= 5.5V, 33.3/17.7 psia	96/264 hrs/0 Fail
Temperature Cycling	JESD22-A104	TC	-65°C to 150°C	500 cycles/0 Fail
Unbiased Temperature/Humidity	JESD22-A102	AC	121°C, 100% RH, 29.7psia	96 hrs/0 Fail
Unbiased Temperature/Humidity	JESD22-A118	UHAST	130°C/110°C, 85% RH, 33.3/17.7 psia	96/264 hrs/0 Fail
Bond Pull Strength	JESD22-B120	BPS	Characterization, Pre Encapsulation	Ppk≥1.66 or Cpk≥1.33
Bond Shear	JESD22-B116	BS	Characterization, Pre Encapsulation	Ppk≥1.66 or Cpk≥1.33
Solderability	M2003 JESD22-B102	SD	Characterization	95% coverage

Note: Either HAST or THB may be chosen. If THB or HAST is run, then UHAST need not be run. Autoclave is not recommended as a qualification test; Unbiased or biased HAST is the recommended stress and is required for organic substrates instead of Autoclave.

5. Reliability Test Results

5.1. Device Reliability Test Results

Stress	Condition	Duration	Sample Size	Result	Classification
ED	Per Datasheet	/	10*3 lot	Pass	/
HTOL	TA = 125°C, V_{cc1}= 5.5V, V_{cc2}= 5.5V	1000 hrs	77*4 lot	Pass	/
ESD-HBM	T_A = 25°C	/	3*1 lot	Pass	Class 3A
ESD-CDM	T_A = 25°C	/	3*1 lot	Pass	Class C3
LU	T_A = 25°C	/	3*1 lot	Pass	Class I A

5.2. Package Reliability Test Results

Package Type: SOIC16-WB							
Stress	**Condition**	**Duration**	**Sample size**	**Results**			
				SFA	**SiMAT**	**UNIMOS**	**JCET**
PC	MSL 3	/	231*3 lot	Pass	Pass	Pass	Pass
HTSL	T_A = 150°C	1000 hrs	77*3 lot	Pass	Pass	Pass	Pass
HAST	130°C, 85% RH, V_{cc1}= 5.5V, V_{cc2}= 5.5V, 33.3psia	96 hrs	77*3 lot	Pass	Pass	Pass	Pass
TC	-65°C to 150°C	500 cycles	77*3 lot	Pass	Pass	Pass	Pass
UHAST	130°C, 85% RH, 33.3psia	96 hrs	77*3 lot	Pass	Pass	Pass	Pass
BPS	JESD22-B120	/	30 bonds/5 ea.	Pass	Pass	Pass	Pass
BS	JESD22-B116	/	30 bonds/5 ea.	Pass	Pass	Pass	Pass
SD	Steam aging, 245°C dipping	5s	22 leads*3 lot	Pass	Pass	Pass	Pass

Package Type: SOIC16-NB						
Stress	**Condition**	**Duration**	**Sample size**	**Results**		
				SFA	**SiMAT**	**JCET**
PC	MSL 3	/	231*3 lot	Pass	Pass	Pass
HTSL	T_A = 150°C	1000 hrs	77*3 lot	Pass	Pass	Pass
HAST	130°C, 85% RH, V_{cc1}= 5.5V, V_{cc2}= 5.5V, 33.3psia	96 hrs	77*3 lot	Pass	Pass	Pass
TC	-65°C to 150°C	500 cycles	77*3 lot	Pass	Pass	Pass
UHAST	130°C, 85% RH, 33.3psia	96 hrs	77*3 lot	Pass	Pass	Pass
BPS	JESD22-B120	/	30 bonds/5 ea.	Pass	Pass	Pass
BS	JESD22-B116	/	30 bonds/5 ea.	Pass	Pass	Pass

SD	Steam aging, 245°C dipping	5s	22 leads*3 lot	Pass	Pass	Pass
Package Type: SSOP16						
Stress	**Condition**	**Duration**	**Sample size**	**Results**		
				池州华宇	**JCET**	
PC	MSL 3	/	231*3 lot	Pass	Pass	
HTSL	T_A = 150°C	1000 hrs	77*3 lot	Pass	Pass	
HAST	130°C, 85% RH, V_{cc1}= 5.5V, V_{cc2}= 5.5V, 33.3psia	96 hrs	77*3 lot	Pass	Pass	
TC	-65°C to 150°C	500 cycles	77*3 lot	Pass	Pass	
UHAST	130°C, 85% RH, 33.3psia	96 hrs	77*3 lot	Pass	Pass	
BPS	JESD22-B120	/	30 bonds/5 ea.	Pass	Pass	
BS	JESD22-B116	/	30 bonds/5 ea.	Pass	Pass	
SD	Steam aging, 245°C dipping	5s	22 leads*3 lot	Pass	Pass	

6. Conclusion

CA-IS37XX series chips are qualified according to JESD47.

Disclaimer

This information is provided to assist customers in design and development. It could change for technology innovation without notice.

The devices are shipped after passing final test. Customers are responsible to conduct sufficient engineering and additional qualification testing to determine whether a device is suitable for use in their applications.

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Revision History

Revision	Change Log	Date
V1.0	Initial release	
V1.1	Re-write with new format	Feb, 2022
V1.2	Add SOIC16-WB JCET/UNIMOS qual results; Add SSOP16 JCET qual results	Jan, 2023
V1.3	Add voltage condition of BHAST & AC	Oct, 2023
V1.4	Add qual lot number	Jan 2024