



Reliability Test Report

Product Name: CA-IF49xx

Report Version: V1.1

Prepared by	Reviewed by	Approved by
邵晓梅	刘和芳	陈亮

Contents

1. Overview.....	3
2. Part Number List	3
3. Product Information	3
3.1. Wafer Information.....	3
3.2. Package Information.....	3
4. Reliability Qualification Plan	4
4.1. Device Qualification Test Requirements.....	4
4.2. Nonhermetic Package Qualification Test Requirements	4
5. Reliability Test Results.....	5
5.1. Device Reliability Test Results	5
5.2. Package Reliability Test Results	5
6. Conclusion.....	6

1. Overview

Reliability testing of microelectronic products is a risk mitigation process designed to ensure the service life of device in customer applications. Semiconductor wafer manufacturing process and package-level reliability can be assessed in a variety of ways and may include accelerated environmental test conditions. Chipanalog evaluates manufacturability of the device to verify a robust silicon and assembly flow to ensure continuity of supply to customers. Chipanalog qualifies new devices, significant changes, and product families based on JEDEC JESD47. CA-IF49xx series chips are packaged with the same wafer. The differences between part numbers are the package and bonding diagram. The data shown is representative of the material sets, processes, and manufacturing sites used by the device family.

2. Part Number List

Package Type	Part Number
SOIC8-NB(S)	CA-IF4988S/CA-IF4905S
MSOP8(M)	CA-IF4905M

Note: JEDEC specification is designed to also qualify a family of similar components utilizing the same fabrication process, design rules, and similar circuits. The family qualification may also be applied to a package family where the construction is the same and only the size and number of leads differs.

3. Product Information

3.1. Wafer Information

Wafer	JUPITER III
Fab Process	18BCD

3.2. Package Information

Assembly site	JCET
FT site	JCET
Package	SOIC8-NB(S)/MSOP8(M)
Lead frame	Cu
Bond wire	20um AuPdCu
MSL level	MSL3

4. Reliability Qualification Plan

4.1. Device Qualification Test Requirements

Stress	Ref.	Abbv.	Conditions	Duration /Accept
Electrical Parameter Assessment	JESD86	ED	Per Datasheet	Per Datasheet
High Temperature Operating Life	JESD22-A108, JESD85	HTOL	$T_J \geq 125^{\circ}\text{C}$ $V_{CC} \geq V_{CCmax}$	1000 hrs/0 Fail
Human Body Model ESD	JS-001	ESD-HBM	$T_A = 25^{\circ}\text{C}$	Classification
Charged Device Model ESD	JS-002	ESD-CDM	$T_A = 25^{\circ}\text{C}$	Classification
Latch-Up	JESD78	LU	Class I or Class II	Classification

4.2. Nonhermetic Package Qualification Test Requirements

Stress	Ref.	Abbv.	Conditions	Duration /Accept
MSL Preconditioning	JESD22-A113	PC	Per appropriate MSL level per J-STD-020	Electrical Test (optional)
High Temperature Storage	JESD22-A103 & A113	HTSL	150°C , 1000 hrs	1000 hrs/0 Fail
Temperature Humidity Bias	JESD22-A101	THB	85°C , 85% RH, V_{CCmax}	1000 hrs/0 Fail
Highly Accelerated Temperature and Humidity Stress	JESD22-A110	HAST	$130^{\circ}\text{C}/110^{\circ}\text{C}$, 85% RH, 33.3/17.7 psia, $V_{cc1} = 5.5\text{V}$, $V_{cc2} = 33\text{V}$	96/264 hrs/0 Fail
Temperature Cycling	JESD22-A104	TC	-65°C to 150°C	500 cycles/0 Fail
Unbiased Temperature/Humidity	JESD22-A102	AC	121°C , 100% RH, 29.7psia	96 hrs/0 Fail
Unbiased Temperature/Humidity	JESD22-A118	UHA	$130^{\circ}\text{C}/110^{\circ}\text{C}$, 85% RH, 33.3/17.7 psia	96/264 hrs/0 Fail
Bond Pull Strength	JESD22-B120	BPS	Characterization, Pre Encapsulation	$Ppk \geq 1.66$ or $Cpk \geq 1.33$
Bond Shear	JESD22-B116	BS	Characterization, Pre Encapsulation	$Ppk \geq 1.66$ or $Cpk \geq 1.33$
Solderability	M2003 JESD22-B102	SD	Characterization	95% coverage

Note: Either HAST or THB may be chosen. If THB or HAST is run, then UHA need not be run. Autoclave is not recommended as a qualification test; Unbiased or biased HAST is the recommended stress and is required for organic substrates instead of Autoclave.

5. Reliability Test Results

5.1. Device Reliability Test Results

Stress	Condition	Duration	Sample Size	Result	Classification
ED	Per Datasheet	/	10*3 lot	Pass	/
HTOL ¹	T _A = 125°C, V _{cc1} = 5.5V	1000 hrs	77*3 lot	Pass	/
ESD-HBM ²	T _A = 25°C	/	3*3 lot	Pass	Class 2
ESD-CDM	T _A = 25°C	/	3*3 lot	Pass	Class C3
LU	T _A = 25°C	/	3*3 lot	Pass	Class 1A

Note1: HTOL test data comes from qualification of CA-IF4988S and CA-IF4905S.

Note2: Test data comes from qualification of CA-IF4988S, CA-IF4905S and CA-IF4905M.

5.2. Package Reliability Test Results

Package Type: SOIC8-WB				
Stress	Condition	Duration	Sample size	Results
PC	MSL 3	/	231*3 lot	Pass
HTSL	T _A = 150°C	1000hrs	77*3 lot	Pass
HAST	130°C, 85% RH, 33.3psia, V _{cc1} = 5.5V, V _{cc2} = 33V	96 hrs	77*3 lot	Pass
TC	-65°C to 150°C	500 cycles	77*3 lot	Pass
UHAIST	130°C, 85% RH, 33.3psia	96 hrs	77*3 lot	Pass
BPS	JESD22-B120	/	30 bonds/5 ea.	Pass
BS	JESD22-B116	/	30 bonds/5 ea.	Pass
SD	Steam aging, 245°C dipping	5s	22 leads*3 lot	Pass

Note: 1 lot package reliability test data comes from qualification of CA-IF4988S, the other 2 lot package reliability data refer to generic data of same package family.

Package Type: MSOP8				
Stress	Condition	Duration	Sample size	Results
PC	MSL 3	/	231*3 lot	Pass
HTSL	T _A = 150°C	1000hrs	77*3 lot	Pass
HAST	130°C, 85% RH, 33.3psia, V _{cc1} = 5.5V, V _{cc2} = 33V	96 hrs	77*3 lot	Pass
TC	-65°C to 150°C	500 cycles	77*3 lot	Pass
UHAIST	130°C, 85% RH, 33.3psia	96 hrs	77*3 lot	Pass
BPS	JESD22-B120	/	30 bonds/5 ea.	Pass
BS	JESD22-B116	/	30 bonds/5 ea.	Pass
SD	Steam aging, 245°C dipping	5s	22 leads*3 lot	Pass

Note: 1 lot package reliability test data comes from qualification of CA-IF4905M, the other 2 lot package reliability data refer to generic data of same package family.

6. Conclusion

CA-IF49XX series chips are qualified according to JEDEC standards.

Disclaimer

This information is provided to assist customers in design and development. It could change for technology innovation without notice.

The devices are shipped after passing final test. Customers are responsible to conduct sufficient engineering and additional qualification testing to determine whether a device is suitable for use in their applications.

License to customers to use the information is limited to the development of applications using the device. Apart from above, the information shall not be reproduced or displayed, and Chipanalog shall not be liable for any claims, compensation, costs, losses or liabilities arising out of the use of the information.

Trademarks

Chipanalog Inc.®、Chipanalog® are trademarks of Chipanalog.

Revision History

Revision	Change Log	Date
V1.0	Initial release	Sep, 2024
V1.1	Add new part number of the same product family	Sep, 2025