Reliability Test Report

Product Name: CA-IF43232EX
Report Version: V1.1

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1. Overview

Reliability testing of microelectronic products is a risk mitigation process designed to ensure the service life of device in customer applications. Semiconductor wafer manufacturing process and package-level reliability can be assessed in a variety of ways and may include accelerated environmental test conditions. Chipanalog evaluates manufacturability of the device to verify a robust silicon and assembly flow to ensure continuity of supply to customers. Chipanalog qualifies new devices, significant changes, and product families based on JEDEC JESD47.

2. Part Number List

Package Type	Part Number
SOIC16-NB(N)	CA-IF43232EN
TSSOP16(TB)	CA-IF43232ETB

Note: JEDEC specification is designed to also qualify a family of similar components utilizing the same fabrication process, design rules, and similar circuits. The family qualification may also be applied to a package family where the construction is the same and only the size and number of leads differs.

3. Product Information

3.1. Wafer Information

Wafer	YALU
Fab Process	18BCD

3.2. Package Information

Assembly site	SiMAT	JCET-D8
FT site	SiMAT	JCET-D8
Package	SOIC16-NB	TSSOP16
Lead frame	Cu	Cu
Bond wire	20um AuPdCu	20um AuPdCu
MSL level	MSL3	MSL3

4. Reliability Qualification Plan

4.1. Device Qualification Test Requirements

Stress	Ref.	Abbv.	Conditions	Duration /Accept
Electrical Parameter Assessment	JESD86	ED	Per Datasheet	Per Datasheet
High Temperature Operating Life	JESD22-A108, JESD85	HTOL	$T_J \geq 125°C$ $V_{CC} \geq V_{CC}$ max	1000 hrs/0 Fail
Human Body Model ESD	JS-001	ESD-HBM	$T_A = 25°C$	Classification
Charged Device Model ESD	JS-002	ESD-CDM	$T_A = 25°C$	Classification
Latch-Up	JESD78	LU	Class I or Class II	0 Fail

4.2. Nonhermetic Package Qualification Test Requirements

Stress	Ref.	Abbv.	Conditions	Duration /Accept
MSL Preconditioning	JESD22-A113	PC	Per appropriate MSL level per J-STD-020	Electrical Test (optional)
High Temperature Storage	JESD22-A103 & A113	HTSL	150°C, 1000 hrs	1000 hrs/0 Fail
Temperature Humidity Bias	JESD22-A101	THB	85°C, 85% RH, V_{CC} max	1000 hrs/0 Fail
Highly Accelerated Temperature and Humidity Stress	JESD22-A110	HAST	130°C/110°C, 85% RH, 33.3/17.7 psia, V_{CC} max	96/264 hrs/0 Fail
Temperature Cycling	JESD22-A104	TC	-65°C to 150°C	500 cycles/0 Fail
Unbiased Temperature/Humidity	JESD22-A102	AC	121°C, 100% RH, 29.7psia	96 hrs/0 Fail
Unbiased Temperature/Humidity	JESD22-A118	UHAST	130°C/110°C, 85% RH, 33.3/17.7 psia	96/264 hrs/0 Fail
Bond Pull Strength	JESD22-B120	BPS	Characterization, Pre Encapsulation	Ppk≥1.66 or Cpk≥1.33
Bond Shear	JESD22-B116	BS	Characterization, Pre Encapsulation	Ppk≥1.66 or Cpk≥1.33
Solderability	M2003 JESD22-B102	SD	Characterization	95% coverage

Note: Either HAST or THB may be chosen. If THB or HAST is run, then UHAST need not be run. Autoclave is not recommended as a qualification test; Unbiased or biased HAST is the recommended stress and is required for organic substrates instead of Autoclave.

5. Reliability Test Results

5.1. Device Reliability Test Results

Stress	Condition	Duration	Sample Size	Result	Classification
ED	Per Datasheet	/	10*3 lot	Pass	/
HTOL	TA = 125°C, V_{cc}= 5.5V	1000 hrs	77*3 lot	Pass	/
ESD-HBM	T_A = 25℃	/	3*1 lot	Pass	Class 2
ESD-CDM	T_A = 25℃	/	3*1 lot	Pass	Class C3
LU	T_A = 25℃	/	3*1 lot	Pass	Class I A

5.2. Package Reliability Test Results

<table>
<tr><th colspan="5">Package Type: SOIC16-NB</th></tr>
<tr><th>Stress</th><th>Condition</th><th>Duration</th><th>Sample size</th><th>Results</th></tr>
<tr><td>PC</td><td>MSL 3</td><td>/</td><td>231*3 lot</td><td>Pass</td></tr>
<tr><td>HTSL</td><td>T_A = 150°C</td><td>1000 hrs</td><td>77*3 lot</td><td>Pass</td></tr>
<tr><td>HAST</td><td>130°C, 85% RH, 33.3psia, Vcc=5.5V</td><td>96 hrs</td><td>77*3 lot</td><td>Pass</td></tr>
<tr><td>TC</td><td>-65°C to 150°C</td><td>500 cycles</td><td>77*3 lot</td><td>Pass</td></tr>
<tr><td>AC</td><td>121°C, 100% RH, 29.7psia</td><td>96 hrs</td><td>77*3 lot</td><td>Pass</td></tr>
<tr><td>BPS</td><td>JESD22-B120</td><td>/</td><td>30 bonds/5 ea.</td><td>Pass</td></tr>
<tr><td>BS</td><td>JESD22-B116</td><td>/</td><td>30 bonds/5 ea.</td><td>Pass</td></tr>
<tr><td>SD</td><td>Steam aging, 245°C dipping</td><td>5s</td><td>22 leads*3 lot</td><td>Pass</td></tr>
<tr><th colspan="5">Package Type: TSSOP16</th></tr>
<tr><th>Stress</th><th>Condition</th><th>Duration</th><th>Sample size</th><th>Results</th></tr>
<tr><td>PC</td><td>MSL 3</td><td>/</td><td>231*3 lot</td><td>Pass</td></tr>
<tr><td>HTSL</td><td>T_A = 150°C</td><td>1000 hrs</td><td>77*3 lot</td><td>Pass</td></tr>
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</table>

Note:

1. Package reliability test of SOIC16-NB(N) comes from 1 lot qualification of CA-IF43232EN and 2 lot generic data of the same package family.
2. Package reliability test of TSSOP16(TB) comes from 1 lot qualification of CA-IF43232ETB and 2 lot generic data of the same package family.

6. Conclusion

CA-IF43232EX series products are qualified with JEDEC standards.

Disclaimer

This information is provided to assist customers in design and development. It could change for technology innovation without notice.

The devices are shipped after passing final test. Customers are responsible to conduct sufficient engineering and additional qualification testing to determine whether a device is suitable for use in their applications.

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Revision History

Revision	**Change Log**	**Date**
V1.0	Initial release	Apr. 2024
V1.1	Add TSSOP16(TB) reliability results	Oct. 2024