AEC-Q100 Qualification Report

Product Series： CA-IS326X-Q1

Report Version： V1.1

Reference Doc.： AEC-Q100-REV-H

Prepare	Review	Approve

Contents

1. Overview

Reliability testing of microelectronic products is a risk mitigation process designed to ensure the service life of device in customer applications. Semiconductor wafer manufacturing process and package-level reliability can be assessed in a variety of ways and may include accelerated environmental test conditions. Chipanalog evaluates manufacturability of the device to verify a robust silicon and assembly flow to ensure continuity of supply to customers. Chipanalog qualifies new devices, significant changes, and product families based on AEC-Q100.

2. Part Number List

Package Type	**Part Number**
MSOW20	CA-IS3265AMT-Q1/ CA-IS3265BMT-Q1/ CA-IS3265CMT-Q1/ CA-IS3265DMT-Q1 CA-IS3266AMT-Q1/ CA-IS3266BMT-Q1/ CA-IS3266CMT-Q1/ CA-IS3266DMT-Q1

Note： AECQ-100 provides the guideline for the use of generic data to accelerate and streamline the qualification process. Products sharing the same major product, process and materials elements may be categorized in a product qualification family.

3. Production Information

3.1. Wafer information

Fab site	SMIC
Wafer	U6Y, X22
Fab Process	18BCD

3.2. Package information

Assembly site	JCET
FT site	JCET
Package	MSOW20
Lead Frame	Cu
Bond wire	20um Au
MSL level	MSL3
Operation Temp.	Grade 1(-40℃ - 125℃)

4. Reliability Qualification Plan

Test Group A–Accelerated Environment Stress Tests					
Group	**Item**	**Refer.**	**Test condition**	**QTY**	**Remark**
A1	PC	J-STD-020 JESD22-A113	Test @ Rm, SMD only, Moisture Preconditioning before THB/BHAST, AC/UHAST, TC, and PTC stress, MSL = 3, Peak Reflow Temp = 260°C	77 pcs*3 lots	
A2	BHAST	JESD22-A110	BHAST: 130°C, 85% RH, Vcc1= 5.5V, Vcc2= 17V, 96 hrs (Test @ Rm/Hot)	77 pcs*3 lots	
A3	UHAST	JESD22-A118	UHAST: 130°C, 85% RH, 96 hrs (Test @ Rm)	77 pcs*3 lots	
A4	TC	JESD22-A104	-65°C-150°C, 500 cycles (Test @Rm/ Hot)	77 pcs*3 lots	
A5	PTC	JESD22-A105	-40°C-125°C, 1000 cycles (Test @ Rm/Hot)	NA	
A6	HTSL	JESD22-A103	T_a = 150°C, 1000 hrs (Test @ Rm/Hot)	45 pcs*1 lot	
Test Group B–Accelerated Lifetime Simulation Tests					
Group	**Item**	**Refer.**	**Test condition**	**QTY**	**Remark**
B1	HTOL	JESD22-A108	T_a = 125°C, V_{cc1}= 5.5V, V_{cc2}= 17V, 1000 hrs (Test @ Rm/Cold/Hot)	77 pcs*3 lots	
B2	ELFR	AEC-Q100-008	T_a = 125°C, V_{cc1}= 5.5V, V_{cc2}= 17V, 48 hrs (Test @ Rm/Hot)	800 pcs*3 lots	
B3	EDR	AEC-Q100-005	Test @ Rm/Hot	NA	
Group C–Package Assembly Integrity Tests					
Group	**Item**	**Refer.**	**Test condition**	**QTY**	**Remark**
C1	WBS	AEC-Q100-001 AEC-Q003	Cpk > 1.67, T0 samples	30 bonds from 5 pcs	
C2	WBP	MIL-STD883 AEC-Q003	Cpk > 1.67, T0 samples	30 bonds from 5 pcs	
C2	WBP	MIL-STD883 AEC-Q003	0 fails, post-TC samples	30 bonds from 5 pcs	
C3	SD	J-STD-002	> 95% coverage, 8hr steam aging prior to testing	15 pcs*1 lot	
C4	PD	JESD22-B100 JESD22-B108 AEC-Q003	Cpk > 1.67	10 pcs*3 lots	
C5	SBS	AEC-Q100-010 AEC-Q003	Cpk > 1.67, 5 balls from min. of 10 devices	10pcs*3 lots	

C6	LI	JESD22-B105	10 leads from each of 5 devices	5pcs*1 lot	
Test Group D–Die Fabrication Reliability Tests					
Group	**Item**	**Refer.**	**Test condition**	**QTY**	**Remark**
D1	EM	JESD61	---	---	Done by Fab
D2	TDDB	JESD35	---	---	Done by Fab
D3	HCI	JESD60 & 28	---	---	Done by Fab
D4	BTI	JESD90	---	---	Done by Fab
D5	SM	JESD61, 87, & 202	---	---	Done by Fab
Group E-Electrical Verification Tests					
Group	**Item**	**Refer.**	**Test condition**	**QTY**	**Remark**
E1	TEST	per datasheet	Pre and Post Stress Electrical Test	All	
E2	HBM	AEC Q100-002	±500V, ±1KV, ±2KV, ±4KV (Test @ Rm/Hot)	3 pcs*1 lot	
E3	CDM	AEC-Q100-011	±250V, ±500V, ±750V, ±2KV (Test @ Rm/Hot)	3 pcs*1 lot	
E4	LU	AEC-Q100-004	125℃, I-trigger ±200mA(Test @ Rm/Hot)	3 pcs*1 lot	
E5	ED	AEC-Q100-009	CPK＞1.67(Test @ Rm/Cold/Hot)	30 pcs*3 lots	
E9	EMC	SAE J1752/3	Electromagnetic Compatibility (Radiated Emissions)	NA	
E10	SC	AEC-Q100-012	/	NA	
E11	SER	JESD89-1/-2/-3	/	NA	
E12	LF	AEC-Q005	/	2 pcs*3 lots	
Group S-Special Requirement Tests					
S1	BLR-Bending	JESD22-B113	Align with customer	NA	
S2	BLR-Drop	JESD22-B11	Align with customer	NA	
S3	BLR-TC	IPC-9701	Refer test requirement	NA	
S4	BLR-Vibration	JESD22-B103	Refer test requirement	NA	

Note: Group E6, E7 and Group F are not reliability related items. Group G are not applicable to non-hermetic packaged devices.

5. Reliability Test Results

Test Group A–Accelerated Environment Stress Test (MSOW20)					
Group	**Item**	**Test Condition**	**QTY**	**Lot NO.**	**Result**
A1	PC	Test @ Rm, SMD only, Moisture Preconditioning before BHAST, UHAST, TC stress, MSL = 3, Peak Reflow Temp = 260℃	240 pcs*3 lots	CA-IS3266AMT-Q1 2426A	Pass
				CA-IS3266BMT-Q1 2426A	Pass
				CA-IS3266CMT-Q1 2426A	Pass
A2	BHAST	130℃, 85% RH, 96 hrs, Vcc1= 5.5V, Vcc2= 17V	80 pcs*3 lots	CA-IS3266AMT-Q1 2426A	Pass
				CA-IS3266BMT-Q1 2426A	Pass
				CA-IS3266CMT-Q1 2426A	Pass
A3	UHAST	130℃, 85% RH, 96 hrs	80 pcs*3 lots	CA-IS3266AMT-Q1 2426A	Pass
				CA-IS3266BMT-Q1 2426A	Pass
				CA-IS3266CMT-Q1 2426A	Pass
A4	TC	-65℃-150℃, 500 cycles	80 pcs*3 lots	CA-IS3266AMT-Q1 2426A	Pass
				CA-IS3266BMT-Q1 2426A	Pass
				CA-IS3266CMT-Q1 2426A	Pass
A6	HTSL	T_a = 150℃, 1000 hrs	50 pcs*1 lot	CA-IS3266AMT-Q1	Pass
Test Group B–Accelerated Lifetime Simulation Tests					
Group	**Item**	**Test Condition**	**QTY**	**Lot NO.**	**Result**
B1	HTOL	T_a = 125℃, 1000 hrs, V_{cc1}= 5.5V, V_{cc2}= 17V, input f = 1kHz	77 pcs*3 lots	CA-IS3265AMT-Q1 2526A	Pass
				CA-IS3266BMT-Q1 2529A	Pass
				CA-IS3266CMT-Q1 2529A	Pass
B2	ELFR	T_a = 125℃, 1000 hrs, V_{cc1}= 5.5V, V_{cc2}= 17V, input f = 1kHz	800 pcs*3 lots	CA-IS3265AMT-Q1 2526A	Pass
				CA-IS3266BMT-Q1 2529A	Pass
				CA-IS3266CMT-Q1 2529A	Pass
Group C–Package Assembly Integrity Tests (SOIC16-WB &SOIC14-WB)					
Group	**Item**	**Test Condition**	**QTY**	**Lot NO.**	**Result**
C1	WBS	Cpk > 1.67, Each bonder used, T0 samples	30 bonds from 5 pcs	CA-IS3266AMT-Q1 2426A	Pass

C1	WBS	0 fails, Each bonder used, post-TC samples	30 bonds from 5 pcs	CA-IS3266AMT-Q1 2426A	Pass
C2	WBP	Cpk > 1.67, each bonder used, T0 samples	30 bonds from 5 pcs	CA-IS3266AMT-Q1 2426A	Pass
C2	WBP	0 fails, Each bonder used, post-TC samples	30 bonds from 5 pcs	CA-IS3266AMT-Q1 2426A	Pass
C3	SD	>95% coverage, 8 hrs steam aging prior to testing	15 pcs*1 lot	CA-IS3266AMT-Q1 2426A	Pass
C4	PD	Cpk > 1.67	10 pcs*3 lots	CA-IS3266AMT-Q1 2426A	Pass
				CA-IS3266BMT-Q1 2426A	Pass
				CA-IS3266CMT-Q1 2426A	Pass

TEST GROUP D–Die Fabrication Reliability Tests

Group	Item	Test Condition	ADDITIONAL REQUIREMENTS
D1	EM	---	The Die Fabrication Reliability Tests are carried out by every fabrication site. The data, test method, calculations and internal criteria are available to the customer upon request.
D2	TDDB	---	
D3	HCI	---	
D4	NBTI	---	
D5	SM	---	

Group E-Electrical Verification Tests

Group	Item	Test Condition	QTY	Lot NO.	Result
E1	TEST	Pre and Post Stress Electrical Test	All	All	Pass
E2	HBM	±500V, ±1KV, ±2KV, (Test @ Rm/Hot)	3 pcs*1 lot	CA-IS3265AMT-Q1 2526A	Class 2
E3	CDM	±250V, ±500V, ±750V, ±1KV (Test @ Rm/Hot)	3 pcs*1 lot	CA-IS3265AMT-Q1 2526A	C3
E4	LU	125℃, I-trigger ±200mA; 1.5 × VmaxSUP or MSV(Test @ Rm/Hot)	3pcs*1 lot	CA-IS3265AMT-Q1 2526A	Class II A
E5	ED	CPK＞1.67， test at room, hot, and cold temperature	30pcs*3lot	CA-IS3265AMT-Q1 2526A CA-IS3265BMT-Q1 2529A CA-IS3265CMT-Q1 2529A	PASS
E9	EMC	Electromagnetic Compatibility (Radiated Emissions)	1 pcs*1 lot	NA	NA
E12	LF	MSOW20	Refer to JCET Tin Whisker report		

6. MTTF&FIT

Supporting Data (Ea = 0.7 eV, Confidence Level = 60%)							MTTF (hrs)	FIT
Test Temp.	Test Voltage	Duration	QTY	Fail QTY	Operation Temp.	Operation Voltage	5.94E7	16.84
125℃	5.5V/17V	1000 hrs	231	0	55℃	5.5V/17V		
125℃	5.5V/17V	48	2400	0	55℃	5.5V/17V		

Note: The FIT data is generated based on Arrhenius model and voltage acceleration model.

7. Conclusion

CA-IS326X-Q1 series products are qualified according to AEC-Q100 standard.

Disclaimer

This information is provided to assist customers in design and development. It could change for technology innovation without notice.

The devices are shipped after passing final test. Customers are responsible to conduct sufficient engineering and additional qualification testing to determine whether a device is suitable for use in their applications.

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Revision History

Revision	Change Log	Date
V1.0	Initial release	Jan, 2026
V1.1	Added part number CA-IS3265DMT-Q1 and CA-IS3266DMT-Q1	Feb, 2026